PATENT SPECIFICATION (11) 1 563 794

1 563 794

(21) Application No. 15127/75 (22) Filed 12 April 1975
(61) Patent of Addition to No. 1 486 774 dated 29 July 1974
(23) Complete Specification filed 9 July 1976
(44) Complete Specification published 2 April 1980
(51) INT. CL.³ H04N 7/00
(52) Index at acceptance
H4F BB D22 D30E D30H D30K D30T1

(72) Inventor KEITH LUCAS

(19)

(54) TELEVISION SYSTEMS

(71) We, INDEPENDENT BROADCASTING AUTHORITY, a British Body Corporate, incorporated by Statute, of 70, Brompton Road, London, SW3 1EY, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

A recent development in television transmission is to employ one or more line times of the field blanking periods for the transmission of digitised data. Using a suitably equipped television receiver, the data may be converted into visual charcters which are displayed upon the screen instead of, or superposed upon, the normal picture. Successful operation of this facility depends upon the reliable reception of the data. Difficulties can occur in a modification of the system in which the data is received on a channel separate from the normal television signal, e.g. a telephone channel.

In the Complete Specification of our Patent Application No. 12686/77 (1,486,774) a divisional of Application No. 36206/77 (1,486,772) we have described and claimed a television receiver system having a parallel binary memory device, a clocking device for actuating the memory device, an input for receiving a demodulated television signal carrying, during picture-free periods thereof, a set of pages of information in the form of characters, represented by serial binary signals provided in a repeated cycle the form of which is such that the characters for the set of pages are received in groups of characters, which groups are received each in a different one of said periods and the whole of the information for the set of pages is received during each occurrence of the cycle, each group as received being preceded by a clock run-in signal, to which the clocking device is responsive for synchronization, followed by a known start code, selector means responsive to page address codes present in the cycle, for selecting a page from the set of pages and routing a group of characters, with conversion from serial binary form to parallel binary form, to the memory device when the preceding known start code is received and the preceding page address code corresponds with the selected page while disregarding groups of characters preceded by a page address code corresponding with a page other than that selected, a reading device operable to read the characters repeatedly from the memory device, a character generator responsive to the characters read by the reading device to provide output signals for visual display, as characters, by an intensity modulated raster, together with or separately from picture signals carried by the said demodulated television signal and an arrangement for optionally routing to the memory device alternative character information received over a separate data channel so that characters derived from the alternative character information can be displayed together with or separately from the said picture signals.

It is an object of the present invention to provide an improvement in or modification of this system.

In accordance with the present invention there is provided a television receiver system according to claim 1 of our Patent No. 1,486,774 having for equalising coded character information in the form of a signal which is expected to consist of a series of pulses which are of equal magnitude and which occur or are absent at time points separated by time intervals T, apparatus comprising delay means operable to provide simultaneously a set of outputs the members of which set represent the re-

ceived value of the signal at a continuous succession of said time points, and means for forming an algebraic sum of the members in which the members are given a varied significance such that the sum attributable to an intermediate member of said set is substantially unaffected by the other members of said set.

A signal comprising data in NRZ form is an example of a signal which is expected to consist of a series of pulses which are of equal magnitude and which occur or are absent at time points separated by time intervals T. By sampling the signal at these time points the presence or absence of a pulse at a possible pulse time may represent a one-bit, and the absence of a pulse a zero-bit, or a binary signal or vice versa.

When the transmission channel has a low band-width and/or a non-linear phase characteristic, the waveform of the received (unequalised) signal differs considerably from the ideal rectangular wave pattern. In fact, the peak amplitude is both preceded and succeeded by a pattern of negative and positive signal levels which, overall, can be significant over a period greater than the sampling period. Under poor conditions, the pattern associated with a given pulse can combine with the patterns associated with nearby pulses (both preceding and succeeding) to produce spurious results on sampling.

Using an apparatus according to the invention with the significance of the members arranged to suit the pulse-response properties of the channel, and sampling regularly at a time interval of T, the effect of pulses preceding and succeeding a pulse being sampled (normally the intermediate member of the set) may be diminished or virtually eliminated.

The required varied significance is readily given to the members of the set by effectively multiplying their values by appropriate coefficients. It is readily arranged that no member is given a significance greater than unity and that one member, usually the said intermediate member, is given a significance of unity so that no multiplying apparatus is required therefor. Muliplication by coefficients of less than unity is simply achieved by potentiometers.

In one form of the apparatus operating with a set of five outputs, the delay means is simply a set of delay lines, an even number of delay lines being preferred. Four delay lines connected in series can give the five outputs, including an undelayed, first, output. The fourth and fifth outputs give two members preceding the third output, and the second and first give two members succeeding the third output.

In another form of the apparatus, at least one output which is to preceed the intermediate member is produced by a digital storage device, conveniently a shift register having one or more outputs. Output members which have been obtained from one or more delay lines are summed with appropriate significance and sliced to yield zero-or one-bits depending upon whether their value reaches a predetermined level (50% for a linear characteristic). The bits are clocked through a shift register to give output members having the desired delay and fed back for summing with output members now coming from the delay line or lines. This use of analog and digital delay devices is attractive because of the rugged reliability and predictability of digital devices and because reducing the requirements for analog delays is conducive to economy. Digital delays cannot be used on the unprocessed signal members which have not been summed because, for the reasons given hereinbefore, the unprocessed signals are unsuitable for direct digitising.

The following description in which reference is made to the accompanying drawings is given in order to illustrate the invention.

Figure 1 shows diagrammatically a pulse of unit height and time duration T and the form of the response F(t) obtained after passage through a channel having a non-linear phase characteristic. As will be seen, the response is significant over a time large compared with T.

Figure 2 shows an apparatus according to the invention in diagrammatic form. Using four analog delay lines fed from an input DD for demodulated data signals in a receiver system according to our said Application five output members are obtained at relative times $t-2T$ to $t+2T$.

These outputs are added together, the first and last pairs being multiplied as shown by coefficients b-2, b-1, b_1 and b_2 as shown to give a combined output $F_E(t)$. By suitable setting of the coefficients, interference from adjacent pulses is substantially avoided.

Figure 3 shows a modified apparatus using two analog delay lines *A* and a multiple output shift register *S* which functions as hereinbefore described.

In the Complete Specification of our Patent Application No. 36206/73 (1,486,772) we have described and claimed a television receiver system having a parallel binary memory device, a clocking device for actuating the memory device, an input for receiving a demodulated television signal carrying, during picture-free periods thereof, a set of pages of information in the form of characters, represented

by the serial binary signals provided in a repeated cycle the form of which is such that the characters for the set of pages are received in groups of the characters, which groups are recived each in a different one of said periods and the whole of the information for the set of pages is received during each occurrence of the cycle, each group as received being preceded by a clock run-in signal, to which the clocking device is responsive for synchronisation, followed by a known start code, selector means responsive to page address codes present in the cycle, for selecting a page from the set of pages and routing a group of characters, with conversion from serial binary form to parallel binary form, to the memory device when the preceding known start code is received and the preceding page address code corresponds with the selected page while disregarding groups of characters preceded by a page address code corresponding with a page other than that selected, a reading device operable to read the characters repeatedly from the memory device, a character generator responsive to the characters read by the reading device to provide character signals for visual display, as characters, by an intensity modulated raster, a text adding device responsive to the picture signal component of the demodulated television signal and the character signals to produce a signal representing the television picture with superimposed characters and controller means operable to selectively provide, as required for display, the character signals alone, the said picture signal component alone, or the output of said text adding device.

WHAT WE CLAIM IS:—

1. A television receiver system according to claim 1 of our Patent No. 1,486,774 having for equalising coded character information in the form of a signal which is expected to consist of a series of pulses which are of equal magnitude and which occur or are absent at time points separated by time intervals T, apparatus comprising delay means operable to provide simultaneously a set of outputs the members of which set represent the received value of the signal at a continuous succession of said time points, and means for forming an algebraic sum of the members in which the members are given a varied significance such that the sum attributable to an intermediate member of said set is substantially unaffected by the other members of said set.

2. A system according to claim 1 in which no member of the set is given a significance greater than unity.

3. A system according to claim 2 in which the intermediate member of the set is given a significance of unity.

4. A system according to any one of claims 1 to 3 having potentiometers for multiplying members by significance coefficients of less than unity.

5. A system according to any one of claims 1 to 4 in which the delay means is a set of delay lines.

6. A system according to claim 5 in which the delay lines are connected in series.

7. A system according to any one of claims 1 to 4 in which at least one output which is to preceed the intermediate member is produced by a shift register or other digital storage device.

8. A system according to claim 7 in which output members obtained from one or more delay lines are summed with appropriate significance, sliced to yield zero - or one - bits, depending upon whether the sum reaches a predetermined level, and the bits are clocked through a shift register to give output members having the desired delay and fed back for summing with output members then coming from the delay line or lines.

9. A television receiver system according to claim 1, substantially as herein-before described and illustrated by reference to the accompanying drawings.

ALAN TROMANS & CO.,
Agents for the Applicants,
7, Seymour Road,
London, N3 2NG.

Printed for Her Majesty's Stationery Office by The Tweeddale Press Ltd., Berwick-upon-Tweed, 1980.
Published at the Patent Office, 25 Southampton Buildings, London, WC2A 1AY, from which copies may be obtained.

1563794 COMPLETE SPECIFICATION
1 SHEET

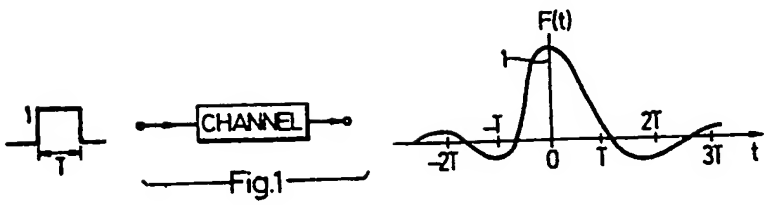

Fig.1

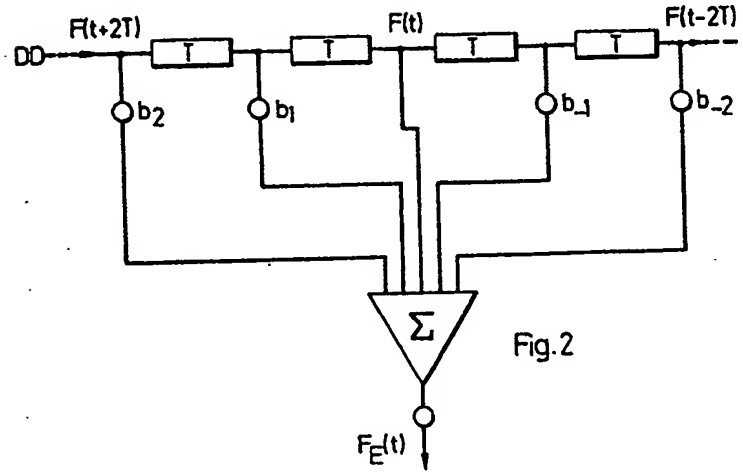

Fig.2

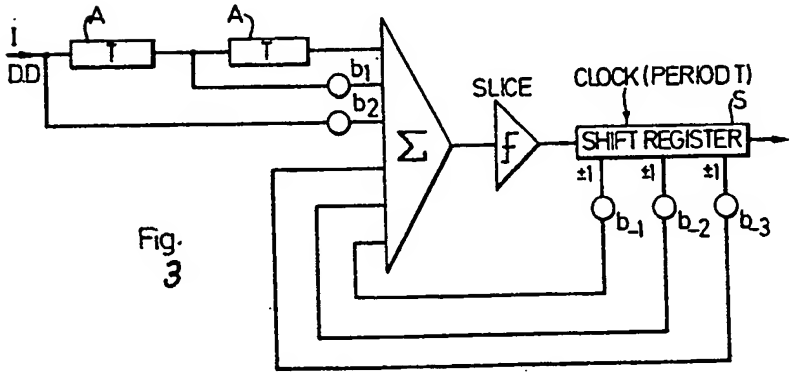

Fig. 3